THE ROLE OF SOLDER IN ADVANCED SEMICONDUCTOR PACKAGING

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A critical aspect of semiconductor fabrication involves the encapsulation of integrated circuits to protect them from physical damage and corrosion, while enhancing their performance and reducing size. The technology around this advanced semiconductor packaging (ASP) is pivotal not only for functionality but also for the economic viability of modern electronic devices.

Here we cover various packaging technologies and methods, including how solder products are integrated into these processes, while shedding light on the evolving convergence between ASP and Surface Mount Technology (SMT).

Types of Advanced Semiconductor Packaging

First, let's explore some of the key types of ASP, including their unique methodologies and applications.

Flip Chip Packaging

Flip Chip Packaging is a method where the semiconductor chip is "flipped" to connect face-down with the substrate or circuit board. This approach allows for shorter interconnections, which are crucial for high-speed, high-performance applications such as smartphones and computing devices. Solder bumping is a common method for creating these connections.

Fan-Out Wafer-Level Packaging (FOWLP)

FOWLP is a cutting-edge technology that offers increased I/O density without the need for interposers or substrates. This method involves expanding the wafer before slicing it into individual chips, which enables more connections per chip. Often, solder balls are formed atop the redistribution layer as the last step before dicing.

System in Package (SiP)

System in Package (SiP) technology encapsulates multiple integrated circuits (ICs) and passive components into a single package, effectively creating a system within a single module. This packaging method allows for significant space savings and enhanced performance by integrating diverse components, such as processors, memory, and sensors, that would typically be spread across a circuit board. As with flip chip packaging, solder bumps may be used to join stacked chips to each other or to the substrate.

Package on Package (PoP)

Package on Package (PoP) is a packaging technique where two or more packages are stacked vertically with solder balls facilitating the inter-package connections. This method is commonly used in mobile devices to save space while increasing functionality by stacking memory chips directly on top of a processor.

3D and 2.5D Packaging

3D packaging involves stacking silicon wafers or dies and interconnecting them vertically using Through-Silicon Vias (TSVs) or other types of connections, which allows for shorter data paths and improved performance. In contrast, 2.5D packaging places

multiple ICs on an interposer (a silicon bridge) that connects to the main substrate. This method facilitates high-speed communication between chips without full vertical integration. Solder microbumps or small solder balls often aid connections.

Chip and Die Connections in Semiconductor Packaging

Die attach is the process of mounting a semiconductor die within a package and establishing a robust mechanical and electrical connection between the die and the substrate. This connection is crucial for the device's thermal management and overall reliability.

Here, we explore the various connection methods, highlighting the role of solder alongside other technologies used in the industry.

Bonding Wire

Bonding wire is a traditional method used to create electrical connections between the semiconductor die and the lead frame or package pins. Typically made from gold, aluminum, or copper, these thin wires are precisely placed to connect tiny bond pads on the die to larger contact points on the package. While effective for many applications, bonding wire can be a limiting factor in miniaturization and is susceptible to mechanical stress.

Sintering

Sintering is a process that uses metal particles to create a robust bond between the die and the substrate without fully melting the materials. This technique is particularly useful in high-power applications where superior thermal and electrical conductivity is crucial. Silver sintering, for example, is favored for its excellent thermal management properties and reliability over traditional solder, especially in high-temperature environments.

Solder

Solder remains one of the most prevalent materials for attaching components in semiconductor packaging. It provides a reliable conductive and mechanical bond at relatively low temperatures. The solder may be jetted, printed, dipped, or placed in the form of solder balls onto a tacky flux before reflow.

Other Adhesives

In addition to metallic bonds, various polymeric adhesives are used in semiconductor packaging. These include electrically conductive adhesives (ECAs) and non-conductive adhesives (NCAs), which are selected based on their thermal, mechanical, and electrical properties. These adhesives are particularly useful in applications where lower temperatures are required during the assembly process, thus preventing damage to sensitive components.

Each connection method has its particular set of advantages and limitations, and often, multiple techniques are used in conjunction to meet the diverse needs of modern electronic devices. For instance, a device may use both solder for board-level attachments and sintering for die attachment to manage thermal loads effectively.

Solder Bumping in Semiconductor Packaging

Solder bumping is a common process in semiconductor packaging that involves placing small solder spheres, or "bumps," onto the contact pads of a chip or wafer. These bumps serve as the connection points between the semiconductor die and the package substrate or another die in stacked configurations.

Bumping often facilitates finer pitch interconnections, which are essential as devices become increasingly miniaturized and complex. Here we detail several key techniques within the solder bumping process.

Wafer Bumping
Wafer bumping involves depositing solder bumps onto the wafer before dicing it into individual dies. This process is integral to flip chip technology, where the die is mounted upside down, and the bumps connect directly to the substrate. Wafer bumping can be executed using several methods:

- Electroplating: A method where solder is electrochemically deposited onto the wafer pad. This technique is highly controlled, allowing for uniform bump heights and compositions, critical for high-density interconnects.
- Stencil Printing: Similar to how solder paste is applied in PCB assembly, stencil printing can be used for wafer bumping. This method is adaptable and cost-effective, suitable for different solder alloys and bump sizes.
- Jetting: An advanced technique that uses a nozzle to deposit solder directly onto the wafer pads. This method offers high precision and is adaptable to various bump sizes.

Copper Pillar Bumping
Copper pillar bumping is a variation of solder bumping that uses a copper post capped with a small amount of solder. This method is increasingly popular for high-performance applications due to the superior electrical and thermal conductivity of copper.

Copper pillar bumps are typically used in conjunction with a micro-bump or interposer technology in 2.5D and 3D IC packaging, where fine-pitch interconnections are necessary. The solder caps in copper pillar bumping are applied using a plating or a print transfer process, ensuring a precise amount of solder on top of each copper pillar.

Scale and Importance
The size of solder bumps can range from larger than 100 microns to less than 10 microns in diameter, addressing various technology needs from basic circuit assembly to advanced chip connections. The scalability of solder bumping techniques allows for their application across a broad spectrum of semiconductor devices, from robust power electronics to delicate wearable technologies.

Solder bumping is critical not only for the physical assembly of semiconductor components but also for ensuring the operational integrity of the device. The mechanical strength, electrical conductivity, and thermal management capabilities of the solder joints are vital for the overall performance and durability of the device.

Convergence of ASP and SMT

As technology evolves, ASP and Surface Mount Technology (SMT) are increasingly converging. This integration poses challenges, such as the need for greater precision and higher thermal management capabilities, but also opens opportunities for streamlined processes and enhanced device reliability.

AIM Solder is at the forefront of this convergence, offering products that support the integration of ASP into traditional SMT lines. We remain committed to supporting our customers with superior solder products and expert technical support, reinforcing our position as a leader in the electronics assembly materials industry.