BACKGROUND

- Customer wanted to investigate cost savings opportunity by using PiP technique

SOLUTION

- 3 phase DOE study was performed to optimize the new PIP process

PHASE 1 | EVALUATE ASSEMBLY

- AIM technical engineers determined if a PiP process could be implemented
- Key considerations evaluated were PCB and component materials, housing design, and PCB layout

PHASE 2 | STENCIL DESIGN

- Several stencil designs were tested to improve overall print performance
- The printing process was evaluated using statistical software and 3D imaging
- Printing results yieled Cpk values over 2 which exceeded the minimum Cpk value of 1.67

PHASE 3 | REFLOW PROFILE OPTIMIZATION

- Two reflow profiles were tested to determine the profile with better performance in terms of PTH barrel fill, voids, solder structure and IMC thickness
- Both the RSS and RTS profile provided solder joints meeting IPC-610G specifications, full barrel fill while producing minimal voids, and IMC layer thickness within the typical tolerances
- Ultimately, the RTS profile was selected to limit the warpage effect on the PCB during reflow

RESULT

- The 3 phase DOE was successfully completed resulting in a ramp up to full scale production
- AIM technical engineers provided hands-on support with the stencil design, print and oven profile optimization
- Customer implemented the PiP process which eliminated the need for costly wave and selective solder applications

An AIM customer approached us for assistance developing a Pin-In-Paste (PiP) process. In close collaboration with AIM's technical engineers, a 3 phase Design of Experiment (DOE) was performed to evaluate and implement the necessary materials and techniques.

Phase 1 - Evaluate PCB assembly features. Determine if a PiP process could be implemented and what input variables would require adjustment.

The key considerations for evaluating an assembly for PiP are:

- PCB materials and components are capable of withstanding high reflow temperatures
- Component design and standoff allow for adequate solder paste flow
- PCB layout allows enough space for required solder paste to be printed on solder mask

Phase 2 - Evaluate/modify stencil design. Design required aperture features in test stencil and run print and reflow trials.

Board and stencil data were reviewed and several PiP aperture design techniques were incorporated into test stencils. (Fig. 1)

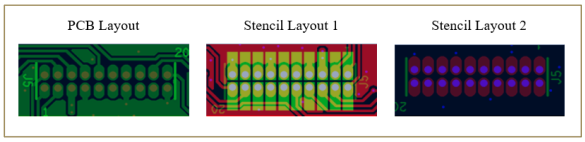

Figure 1. PCB and stencil designs for Phase 1 of DOE.

Phase two of the DOE was conducted to test printing performance. The printing process was evaluated using statistical information generated by the solder paste inspection (SPI) machine.

Controlling paste volume is critical in the PiP process. Balancing the large volume of solder paste needed for PiP apertures against fine pitch print requirements can present significant challenges.

Both stencil aperture design and printer settings can be adjusted to achieve the desired outcome. These include step stencils and off-contact printing.

A minimum C_{pk} of 1.67 (99.977% yield) a 5-sigma printing process was required. Twenty-five (25) PCBs using two different stencil designs resulted in C_{pk} over 2.0 for paste area, height, and volume, exceeding their minimum requirements.

Printer settings in Table 1 produced the best results.

Optimal Print Parameters	
Print Pressure (kg)	9.6
Print Speed (mm/s)	75.0
Separation Speed (mm/s)	7.0

Table 1

Component placement/insertion also requires consideration. Lead-to-hole ratios must be wide enough to allow for solder to flow between the pin and the barrel and to allow for insertion tolerance. However, they can't be so wide so that molten solder runs out before the solder can wet and solidify completing the connection. PCB surface finish and component lead forming capabilities can also influence the process window. Finally, minimizing solder paste displaced during the insertion process needs to be accomplished. The solder paste formulation must be tested to ensure the paste can accommodate requirements unique to the PiP process.

Phase 3 - Optimize the reflow profile.

Phase three involved processing the boards using two reflow profiles to analyze PTH barrel fill, voids, solder joint structure and IMC thickness. The profiles tested were typical ramp-to-spike (RTS) and ramp-soak-spike (RSS) profiles.

Each profile has advantages depending on the application. RTS reduces thermal exposure of the assembly reducing oxidation of paste deposits and wetted surfaces, minimizes material deformation and reduces profile length. RSS is implemented to minimize ΔT of a palletized, thermally massive or mismatched assembly.

Profiling for a PiP process may require unconventional adjustments. As previously mentioned, ensuring paste and molten solder stay in the through-hole aperture is necessary and reflow profiles can be manipulated to compensate for sub-optimal board design, aperture design, and lead-to-hole ratio.

Excess solder paste residue can be an issue with PiP processes due to the large volume of paste required to achieve barrel fill. Excess residue can interfere with post-reflow processes such as pin-testing and coating application. It can also adversely impact oven flux management systems and oven cleaning schedules.

These conditions should be monitored as a process is brought to production scale to ensure there are no unexpected issues.

Profiles were optimized and compared to determine which profile produced the best results. Both profiles produced solder joints meeting IPC-610G specifications. X-ray inspection and cross section analysis revealed >100% barrel fill and minimal voids. Microscopy showed good wetting and intermetallic thickness.

Ultimately, the RTS profile (Table 2) was selected as it reduced PCB warping. PCB planarity was an important consideration to ensure connectors were properly aligned and oriented.

RTS Profile Parameters			
Peak Temperature	241°C	Time Above Liquidus (TAL)	30 seconds
Ambient to Peak	3.5 seconds	Rising Slope	1.8°C/seconds

Table 2

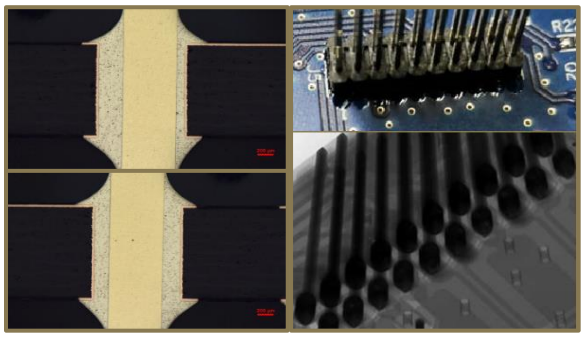

Figure 2. RTS profile produced IPC-610G compliant solder joints with full barrel fill and minimal voids on PiP components.

The newly developed PIP process was ramped to a full production scale with complete success.

AIM engineers provided hands-on support with stencil design, print and oven profile optimization. AIM's technical staff is highly proficient within all facets of PCB assembly to assist in implementation of new processes or to optimize existing programs.

Effectively implementing the PiP technique allowed the customer to save money by eliminating the need for a wave, selective or manual soldering process.